Application No. 09/591,044
Filed: June 9, 2000
TC Art Unit: 2112
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AMENDMENT TO THE CLAIMS

1. (currently amended) A system for transferring data between a plurality of devices coupled to a bus, at least one of the plurality of devices being operative at a plurality of clock rates, comprising:

a bus including ~~at least one~~ a data line ~~for transmitting the~~ operative to carry data and ~~at least one~~ a clock line operative to carry a clock signal; and

~~at least one~~ first and second ~~device~~devices ~~communicably~~operatively coupled to the bus, at least the second device including at least one data register,

wherein the first and second ~~device~~ devices ~~is~~ are operative at a first clock rate, and the second device is further operative ~~and~~ at a second reduced clock rate, the second reduced clock rate being less than the first clock rate,

wherein at least the first device is operative to transmit data over the data line, and

wherein the ~~first~~ second device is operative to receive at least a portion of the data transmitted over the data line, ~~and~~ to store the at least a portion of the data in ~~a~~ the data register, and, in the event the first device is operating at the first clock rate and the ~~first~~ second device is operating at the second

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reduced clock rate, to drive the clock line to a ~~first~~ predetermined logic level while the data is stored in the data register, thereby enabling data transfer between the first device and ~~at least one~~the second device over the bus while the ~~first~~ second device operates at the second reduced clock rate.

2. (currently amended) The system of claim 1 wherein the ~~first~~ second device is further operative at least at the second reduced clock rate to clear the data from the data register upon completion of the data transfer.

3. (currently amended) The system of claim 1 wherein the second device further ~~including~~ includes ~~pull up~~control circuitry for ~~pulling~~ driving the clock line to ~~a~~ the ~~second~~ predetermined logic level~~,~~ and ~~wherein the first device is further operative to release~~for releasing the clock line upon completion of the data transfer~~ to allow the clock line to be pulled to the second predetermined logic level by the pull-up circuitry~~.

4. (canceled)

5. (canceled)

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6. (currently amended) A method of transferring data between a plurality of devices coupled to a bus, at least one of the plurality of devices being operative at a plurality of clock rates, comprising the steps of:

providing first and second devices coupled to a bus, at least the second device including a data register, the bus including a data line for carrying data and a clock line for carrying a clock signal;

operating the first device at a first clock rate and operating the second device at a second reduced clock rate, the second reduced clock rate being less than the first clock rate;

transmitting data over the data line by the first device;

receiving at least a portion of the data transmitted over the data line by the second device;

storing at least a portion of the data transmitted over the data line in ~~a~~ the data register by ~~at least one~~the ~~first~~ second device ~~communicably coupled to a bus, the bus including at least one data line for transmitting the data and at least one clock line, the first device being operative at a first clock rate and at a second reduced clock rate, the reduce clock rate being less than the first clock rate~~; and

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~~in the event the first device is operating at the reduced clock rate,~~ driving the clock line to a ~~first~~ predetermined logic level while the data is stored in the data register by the ~~first~~ second device, thereby enabling data transfer between the first device and ~~at least one~~the second device over the bus while the ~~first~~ second device operates at the second reduced clock rate.

7. (currently amended) The method of claim 6 further including the step of clearing the data from the data register upon completion of the data transfer by the ~~first~~ second device.

8. (currently amended) The method of claim 6 wherein the driving step includes driving the clock line ~~is pulled~~ to ~~a~~ the ~~second~~ predetermined logic level by ~~pull-up~~control circuitry included in the second device, and further including the step of releasing the clock line upon completion of the data transfer by the ~~first device~~control circuitry within the second device, ~~thereby allowing the clock line to be pulled to the second predetermined logic level by the pull-up circuitry~~.

9. (canceled)

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